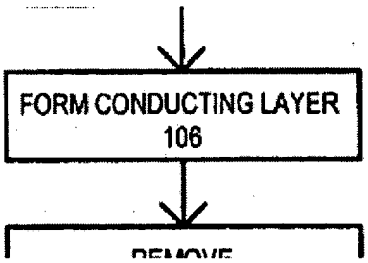
E. Remarks

Rejections Under 35 U.S.C. §112, First Paragraph.

The rejection argues that the Specification fails to enable certain features of Applicants' claim. With respect to claim 1, the following is argued:

> In the specification, the applicant discloses the step of depositing the conductive layer over the stop layer and the step of removing the conductive layer to form and interconnection using the stop layer as removal stop. However, applicants do not disclose how to form the conductive layer in claim 1. Applicants do not disclose either the location of the conductive layer and the conductive layer removal step. (Office Action, dated 9/21/04, Page 2, Last full paragraph).

Applicants believe particular examples of the above noted limitations are shown in the Specification. Disclosure showing the formation of a conductive layer is shown in multiple places within Applicants' Specification. A first location supporting these limitations appears in FIGS. 1 and 2C, and the corresponding written description:



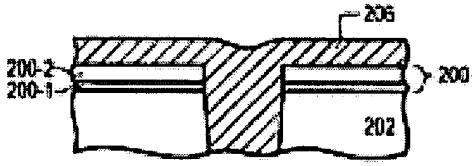
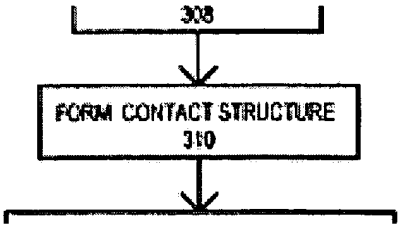


FIG. 2C

> Once a contact hole **204** has been opened, a conducting layer may be formed (step **106**). As shown in FIG. 2C, a conducting layer **206** may fill a contact hole **204**, and may also be formed over a composite layer **200**. (Specification, Page 9, Lines 2-4).

A second location supporting these limitations appears in FIGS. 3 and 4E, and the corresponding written description:



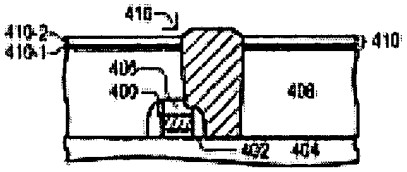


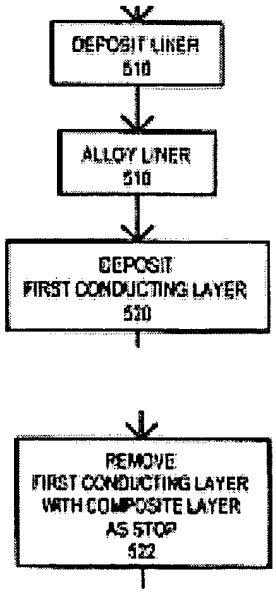
FIG. 4E

Following the formation of a contact hole **414** with a composite layer **410** as a hard etch mask, a contact structure may be formed (step **310**). FIG. 4E shows a contact structure **416** formed within a contact hole **414**. A contact structure **416** may include a conductive material and provide a conductive path between a substrate **404** and a subsequently formed conductive layer.

It is understood that while FIG. 4E illustrates a self-aligned contact to a substrate **404**, a second embodiment may include other such contacts. Self-aligned contacts may be made to thin film transistors instead of transistors formed in a bulk silicon substrate, to name but one example.

It is also understood that a contact structure **416** may be formed in a variety of ways. To name but two examples, a conducting layer may be deposited and then patterned, or a conducting layer may be deposited and then chemically-mechanically polished and/or etched back to form a "plug" contact structure. (Specification, Page 11, Lines 2-14).

A third location supporting these limitations appears in FIG. 5 and (newly submitted) FIGS. 6H to 6J, and the corresponding written description:



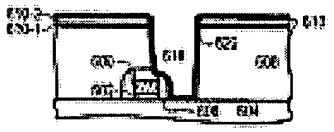


FIG. 6H

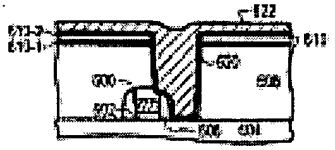


FIG. 6I

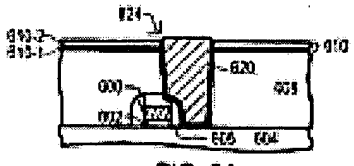


FIG. 6J

> In the particular method of FIG. 5, a conducting "liner" may be deposited (step **516**). A conducting liner may be a material, or combination of materials, that can provide a diffusion barrier for a subsequently deposited material and/or provide a conductive layer that adheres to lower layers. A step **516** may include sputtering a layer of titanium (Ti), followed by a layer of titanium nitride (TiN), as just one example. FIG. 6H shows an integrated circuit following a conducting liner deposition. A conducting liner **620** may be formed over a composite layer **610** and into a contact hole **618**, including an exposed portion of a substrate **604**. A conducting liner **620** may then be alloyed to a substrate (step **518**).
>
> A first conducting layer may then be deposited (step **520**). As shown in FIG. 6I, a first conducting layer **622** may fill a contact hole **618** and be formed over a composite layer **610**. A first conducting layer **622** may include tungsten (W). A tungsten layer may be deposited with plasma vapor deposition (PVD) or CVD techniques using silane and tungsten hexaflouride (WF_6) as reactant gases, as just two examples.
>
> Portions of a first conducting layer may then be removed with a composite layer as a stop (step **522**). In the particular arrangement of FIG. 6J, a step **522** may include a CMP step. With composite layer **610** functioning as a stop, first conducting layer **622** may be removed exposing a composite layer **610** and forming a "plug" contact structure **624**. (Specification, Page 16, Lines 3-19).

All of the above examples clearly show how a conductive layer can be formed, as well as the location of such a conductive layer.

Of course, Applicants stress that the above are particular embodiments provided in support of claim limitations, and should not be construed as representing Applicants' claim limitations.

With respect to claim 11, the rejection argues that the Specification does not enable "forming a conducting interconnect structure after removing a first conductive layer" as "it is impossible to remove a 'first conductive layer' without knowing the location of the first conductive layer. Applicants believe the above argument with respect to claim 1 illustrates how support may also be found for the limitations of claim 11.

Rejections of Claims 3-5, 13-14 and 17-18 Under 35 U.S.C. §112, Second Paragraph.

Claim 3 has been amended to overcome the rejection.

Claims 13 and 17 have been amended to overcome the grounds for rejection.

Rejection of Claims 1, 8-9, 11-13, 15 and 17-18 Under 35 U.S.C. §102(e) based on *Jang et al.* (U.S. Patent No. 5,840,624).

The rejection of claims 1 and 8 will first be addressed.

The invention of amended claim 1 is directed to a method that includes forming a stop layer, forming a contact with chemical-mechanical polishing that removes a conductive layer

with the stop layer as a conductive layer removal stop, and performing a borderless contact etch with the stop as an etch stop in the borderless contact etch.

Claim 1 has been amended to include the limitations of dependent claim 7. The rejection has indicated the limitations of claim 7 were not shown by the single reference *Jang et al.*[1] Accordingly, this ground for rejection is traversed.

The rejection of claims 9 and 11-13 will now be addressed.

Amended claim 9 is directed to a method that includes removing a first conducting layer formed over a stop layer having a contact hole formed therein, with the stop layer as a removal stop, to form a contact structure. The method also includes forming a conducting interconnect structure after removing a first conducting layer, the conducting interconnect structure contacting the contact structure. In addition, a borderless contact pattern is etched into an insulating layer formed over the stop layer, with the stop layer as an etch stop. The borderless contact pattern exposes at least a portion of the conducting interconnect structure.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.

Jang et al. teaches the reduction of via overetching for borderless contacts. The reference teaches a metal structure 22 as well as a second via hole 25. Such structures are argued to correspond to Applicants' claim limitations as follows:

> Jang discloses... removing the first conductive layer (22)... forming a conducting interconnect structure (22) after removing the conductive layer (Fig 6)... the interconnection structure contacts with the contact structure (Fig 8). (Office Action, dated 9/21/04, Page 4, Section 6).

Applicants note that the above rationale presents a contradiction in terms. As emphasized above, Applicants' amended claim 9 recites:

[1] Office Action, dated 9/21/04, Page 7, Lines 14-16.

"forming a conducting interconnect structure after removing the first conducting layer".

However, the rejection argues that the same structure of *Jang et al.* (metal structure 22) corresponds to both the "interconnect structure" and the "first conducting layer". Thus, the reference cannot show Applicant's claim 9 limitations, as under such an interpretation, the same structure is formed after it is removed.

For this reason, the cited reference does not show all of Applicants' claim limitations, and this ground for rejection is traversed.

The rejection of claims 15 and 17-18 will now be addressed.

The invention of amended claim 15 is directed to a method that includes forming a stop layer between a first insulating layer and a second insulating layer. The stop layer has a substantially slower removal rate than a conducting material in a step that removes essentially all of the conducting material above a top surface of the stop layer and retains the conducting material below the top surface of the stop layer to form a contact in the first insulating layer. In addition, the stop layer has a substantially slower removal rate than the second insulating material in an etch step that forms a borderless contact pattern in the second insulating layer.

As noted above, the reference *Jang et al.* teaches a metallization layer (not shown or numbered in the reference) formed over a layer of silicon nitride 20 (argued to correspond to Applicants' stop layer). The metallization layer is etched to form a metal structure 22. However, as shown in FIG. 6, the metal structure 22 is not removed above the nitride layer 20, but rather retained for subsequent contact with "intentional" borderless contact metal structure 27.

Accordingly, because the cited reference does not show all the limitations of amended claim 15, this ground for rejection is traversed.

Rejection of Claims 2-3, 6 and 14 Under 35 U.S.C. §103(a), based on *Jang et al.* in view of *Inou et al.* (U.S. Patent No. 5,604,374).

The rejection of claims 2-3 and 6 will first be addressed.

Claim 2 depends from claim 1. Claims 3 and 6 depend from claim 2.

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference

teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[2]

To the extent that this ground for rejection relies on *Jang et al.*, the comments set forth above for claim 1 are incorporated herein. Namely, *Jang et al.* does not teach chemical-mechanical polishing to remove a conductive layer with a stop layer as a conductive layer removal stop. Likewise, *Inou et al.* is silent as to such a limitation. Accordingly, the combination of references does not show, and is not believed to suggest all the limitations of claim 1, and a prima facie case of obviousness does not exist. For this reason, this ground for rejection is traversed.

The rejection of claim 14 will now be addressed.

Claim 14 depends from claim 12. Thus, to the extent that this ground for rejection relies on *Jang et al.*, the comments set forth above for claims 9 and 11-12 are incorporated herein. Namely, that *Jang et al.* does not show "forming a conducting interconnect structure after removing the first conducting layer". *Inou et al.* provides no teaching with respect to an interconnect structure, as this reference is directed to the formation of a bipolar transistor. Accordingly, the combination of references does not show, and is not believed to suggest all the limitations of claim 12, and a prima facie case of obviousness does not exist. For this reason, this ground for rejection is traversed.

Rejection of Claims 4-5 Under 35 U.S.C. §103(a), based on *Jang et al.* in view of *Inou et al.*, further in view of *Hedge et al.* (U.S. Patent No. 5,604,374).

Claims 4 and 5 depend from claim 2.

To the extent that this ground for rejection relies on *Jang et al.*, the comments set forth above for claim 2 are incorporated herein. Namely, *Jang et al.* in view of *Inou et al.* is believed to show or suggest all the limitations of claim 1.

Hedge et al. shows the formation of a conductive structure used in a dual inlaid damascene process. In the arrangement shown, etch stop layers (112 and 116 separate dielectric layers). However, such layers are never used as a "conductive layer removal stop" in a chemical-mechanical polishing step.

[2] MPEP §2143.

Accordingly, the combination of references is not believed to show or suggest the limitations of base claim 1, and a prima facie case of obviousness has not been established.

Rejection of Claims 7, 10 and 16 Under 35 U.S.C. §103(a), based on *Jang et al.* in view of *Liaw* (U.S. Patent No. 6,448,140).

As noted above, claim 1 has been amended to include the limitations of dependent claim 7. Accordingly, the limitations of claim 1 will be addressed in this section.

The rejection of claim 1 will first be addressed.

The invention of amended claim 1 is directed to a method that includes forming a stop layer, forming a contact with chemical-mechanical polishing that removes a conductive layer with the stop layer as a conductive layer removal stop, and performing a borderless contact etch with the stop as an etch stop in the borderless contact etch.

To show the limitations of amended claim 1, the rejection proposes modifying *Jang et al.* in view of *Liaw*:

> Jang clearly discloses using RIE to create the contact... Liaw discloses using either chemical mechanical polishing (CMP) or RIE to create the contact structure (col. 6 lines 16-30). It would have been obvious... to modify Jang in view of Liaw by using CMP to create a contact because equivalent and substitution of one for the other would produce an expected result. (Office Action, dated 9/21/04, Page 7, Lines 15-20).

Applicant's respectfully disagree, and believe that the proposed modification is not obvious.

As is well settled, if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.[3]

Including a CMP step to remove the metal structure (22) of *Jang et al.* would make the resulting structure unsuitable for its intended purpose. First, *Jang et al.* teaches the use of RIE in combination with photolithography to define a metallization layer to thereby form metal structure (22):

> ***Photolithographic and*** RIE procedures, again using Cl_2 as an etchant are used to define metal structure, 22, shown schematically in FIG. 6. (*Jang et al.*, Col. 5, Lines 26-28, emphasis added).

The resulting metal structure 22, as shown in FIG. 8 of *Jang et al.*, extends above the insulating layer upon which is was formed

In sharp contrast, *Liaw* teaches a metal removal step performed without lithography to remove a metal from a top surface of an insulating layer, as shown and described with reference to FIG. 7 of *Liaw*:

> After removal of photoresist shape 13... SAC structure 15, can be comprised of a refractory metal such as tungsten, or of an aluminum based layer. After metal deposition... a chemical mechanical polishing, (CMP), procedure, or a selective RIE procedure, using Cl_2 as an etchant, is used to ***remove unwanted regions of metal*** from the top surface of ILD layer 12... (*Liaw*, Col. 6, Lines 14-27).

That is, the two steps of the references are not equivalent, as *Jang et al.* teaches patterning a metallization layer to define a metal structure that resides on the top of an insulating layer, while *Liaw* teaches removing a metal layer from the top of an insulating layer.

The non-equivalence between such steps is best shown by referring to FIG. 8 of *Jang et al.* If metal structure 22 were removed from the surface of nitride layer 20, metal structure 27 would either fail to make contact with metal structure 22, or produce a defective, high resistance contact.

Thus, because the proposed modification would render the reference *Jang et al.* unsuitable for its intended purpose, the necessary motivation for the proposed combination is believed to be lacking, and a prima facie case of obvious has not been established for these claims.

The rejection of claims 10 and 16 will now be addressed.

---

[3] In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984).

Claim 10, which depends from claim 9, recites that removing a first conducting layer includes chemical-mechanical polishing. Claim 16, which depends from claim 15, recites that a material removal step includes chemical-mechanical polishing.

To address this ground for rejection Applicants incorporate by reference herein the comments set forth above for claim 1. In particular, motivation for the proposed combination is believed to be lacking.

Rejection of Claim 19 Under 35 U.S.C. §103(a), based on *Jang et al.* in view of *Yoshida et al.* (U.S. Patent No. 6,255,700).

Claim 19, which depends from claim 15, recites that a first insulating layer includes silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

To the extent that this ground for rejection relies on *Jang et al.*, the comments set forth above for claim 15 are incorporated herein. Namely, *Jang et al.* is not believed to show or suggest all the limitations of claim 1.

In addition or alternatively, Applicants believe that the rejection does not presented a prima facie case of obviousness for additional reasons.

As is well settled, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found in either the references themselves or in the knowledge generally available to one of ordinary skill in the art.

The rejection relies on the following rationale to modify *Jang et al.* in view of *Liaw*:

> It would have been obvious... to use PSG having a concentration greater than 5-wt% because this would enhance the etching of the insulating layer. (Office Action, dated 09/21/04, Page 8, Lines 5-8).

Applicants have reviewed the reference *Yoshida et al.* and have found no teachings regarding an enhancement of etching arising from utilizing phosphosilicate glass (PSG). Therefore, the above teaching is not from the reference itself.

If the examiner is taking official notice with respect to this teaching, Applicants seasonably traverse such notice and request a reference in support. The invention of claim 19 recites phosphorous doped silicon oxide in combination with the recited stop layer utilized as

both a layer removal stop and borderless contact etch stop. Thus, a supporting reference would have to teach why highly doped PSG is desirable in such an arrangement.

In addition, the term "enhance" is unclear. If by enhanced the rejection means "faster" or "more selective", Applicants readily admit that according to some etching techniques, PSG will etch at a faster rate than non-doped silicate glass (NSG) or silicon nitride, but such effects are entirely dependent upon the process employed as well as the surrounding structures. Thus, Applicants cannot agree that the general knowledge indicates that highly doped (e.g., greater than 5-wt%) PSG always presents an "enhanced" etching effect. In fact, *Yoshida et al.* indicates PSG presents a distinct drawback in some applications:

> When increasing the phosphorus concentration, however, a problem occurs that the phosphorus in the inter-layer insulating film PSG 20 diffuse in the high-resistance polysilicon 8 to decrease the resistance value of the high-resistance polysilicon 8. (*Yoshida et al.*, Col. 4, Lines 18-22).

For the above reasons, Applicants do not believe that the suggestion/motivation relied upon to combine the cited reference is present in the references themselves or general knowledge of those skilled in the art. Accordingly, the necessary motivation/suggestion for a prima facie case of obviousness has not been established, and this ground for rejection is traversed.

Rejection of Claim 20 Under 35 U.S.C. §103(a), based on *Jang et al.* in view of *Yoshida et al.*, further in view of *Inou*.

Claim 20, which depends from claim 19, recites that the stop layer includes a layer of substantially undoped silicon dioxide.

To the extent that this ground for rejection relies on the combination of *Jang et al.* in view of *Yoshida et al.*, the comments set forth above for claim 19 are incorporated by reference herein. In particular, the references do not show all the limitations of base claim 15, and the requisite motivation for combining the reference is believed to be lacking.

Claims 1, 3-5, 9, 13, 15 and 17 have been amended. Claims 7 and 11-12 have been cancelled. Claims 3-5, 13 and 17 have been amended not in response to the cited art, but to clarify claim terms and correct claim dependencies.

The present claims 1-6, 8-10 and 13-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

12/16/04

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D. Amendments to the Figures.

New FIGS. 6G to 6L are included herewith. These figures show material disclosed in the present Specification as well as the original provisional application. In particular, the information of FIGS. 6G to 6L is included in the Specification at Page 15, Line 20 to Page 17, Line 6. Thus, FIGS. 6G to 6L represent information contained in the Specification that has been added to the figures. This does not present new matter:

> Stated another way, information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter. (MPEP §2163.06).

FIGS. 7A to 7K have been amended to include the label "BACKGROUND ART".